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XS9922B Datasheet

4Ch HD/SD Analog Video Decoder

Version: V1.0

2023-5-5

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1 Preface

1.1 Description

XS9922B includes 4-channel Analog Video Decoder with MIPI-CSI2 interface. It delivers CVBS, 1M, 2M image. It receives CVBS, Universal 1M, 2M analog video input from Camera and the other video signal sources. It accepts Single-ended analog SD/HD/FHD video signals, and then Processing Clamp/AGC/YC Separation and Converting MIPI-CSI2 format. MIPI-CSI2 interface compliant with MIPI-DPHY v1.1.

XS9922B integrate high performance Audio Codec, which includes 3-channel MIC input, 2-channel LineIn input and 1-channel LineOut output. Audio Codec supports Voice Acquisition, Voice Intercom, and other voice application.

XS9922B support Coaxial Communication Protocol communicates between controller(DVR) and Camera on the video signal through coaxial cable.

1.2 Product Version

Product Name	Version
XS9922B 4-CH HD/SD Analog Video Decoder	V1.0

1.3 Intended Audience

This document is intended for:

- Design and maintenance personnel for electronics
- Sales personnel for electronic components

1.4 Revision Record

Date	Version	Description	Note
2023-5-5	V1.0	Initial	-

CONTENTS

FIGURES

TABLES

2 Product Overview

2.1 Application Scenario

XS9922B is RX chip with 4-channel Analog Video Decoder. It accepts HDCCTV and CVBS analog video input and converts MIPI CSI-2 format. The following diagram shows the application scenario.

XS9922B accepts and decodes composite analog video signals, and converts to MIPI CSI-2 format video data to Encoder Chip. This system can implement video preview, video storage and other functions.

Encoder Chip can access XS9922B via IIC interface.

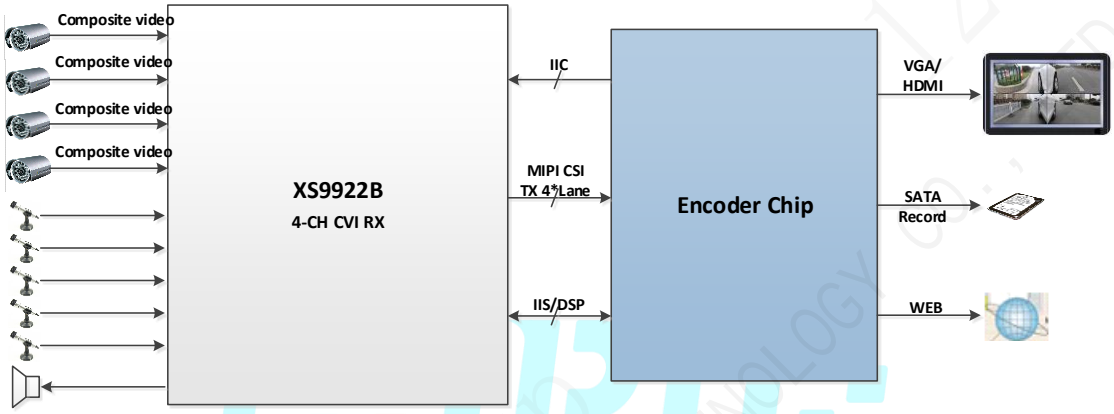


Fig. 2-1 XS9922B Application Scenario

2.2 Functional Block Diagram

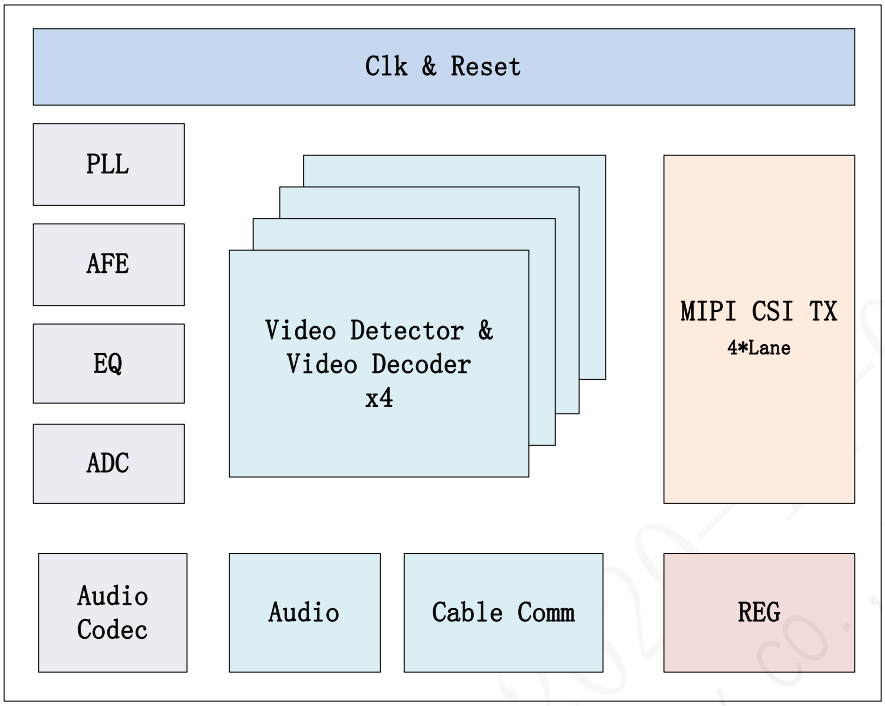


Fig.2-2 XS9922B Functional Block Diagram

2.3 Features

- Input
  - 4-CH single-ended composite analog video signals Input
    - HDCCTV 1M/2M
    - CVBS

Table 2-1 XS9922B HDCCTV video format

	720P	1080P
HDCCTV	25F(16:9) 30F(16:9) 50F(16:9) 60F(16:9)	25F(16:9) 30F(16:9)

- Output
  - Support MIPI CSI-2, 4 Lane interface
  - MIPI CSI-2 1/2/3/4 Data Lane configuration
  - Support Max 1.5Gbps/Lane
  - Support YUV 422 8-bit data format
  - Support Max 4 Virtual Channels
    - 2 Data Lane for up to 720p@50/60, 1080P@25/30 2-CH
    - 4 Data Lane for up to 720p@50/60, 1080P@25/30 4-CH
- Image Signal Processor
  - Support single-ended analog video input up to 2M format for each CH
  - On-Chip Analog Clamp/EQ
  - Accept CVBS D1/960H, 720P@25F/30F/50F/60F, 1080P@25F/30F
  - Auto-detection for different video format
  - Robust sync detection for video signals
  - Programmable Brightness, Contrast, Saturation and Hue
  - Robust color carrier frequency offset compensation
  - High-performance Y/C separation filter
  - Support AGC, ACC and White Peak
  - Support LTI and CTI
- Audio
  - Support audio transmission via coaxial cable. Audio supports 16bit/8KHz, 16bit/16KHz sample rate
  - Integrated high-performance Audio Codec, which includes 3-CH LineIn/MIC, 2-CH LineIn, and 1-CH LineOut
  - Audio Codec supports 8K/16K/32K/44.1K/48K sample rate, and 16/20/24bit sample accuracy
  - SNR > 95dB, THD < -80dB for audio sampling
  - Embedded 2-CH IIS interface, one for audio recorder, the other for audio playback
  - IIS supports 8K/16K/32K/44.1K/48K sample rate, and 16/20/24bit sample accuracy

- Support audio cascading of up to 4 chips

◆ Other

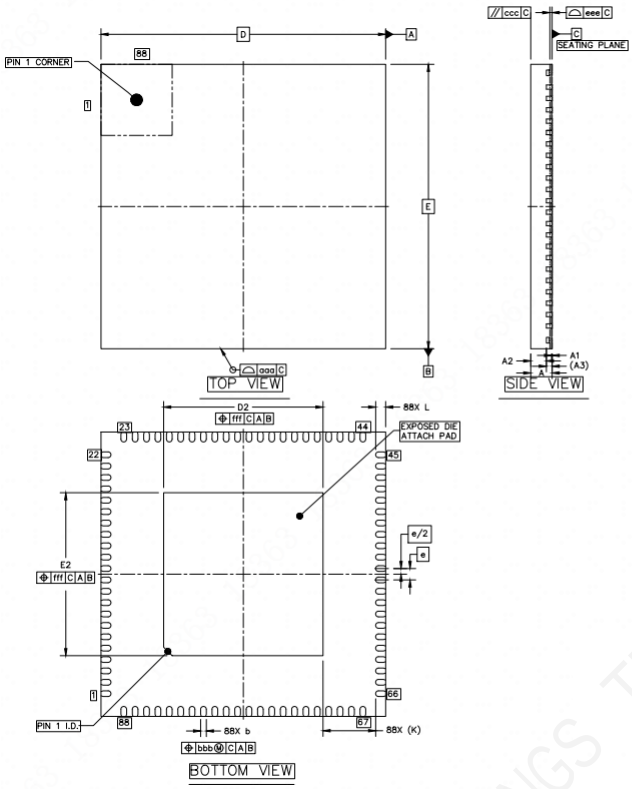
- Support flexible mapping between video inputs and video outputs
- 4-CH PTZ for 4-CH video channel, communicating with remote Camera device
- Embedded IIC slave of 100Kbps~400Kbps rate
- Support interrupt output for video loss and remote communication
- Single 27MHz Crystal input, built-in PLL
- 3.3V/2.5V/1.1V Supply Voltage
- 88 pin QFN package

3 Hardware

3.1 Package and PIN

3.1.1 Package(QFN88)

XS9922B uses QFN88 package. Its dimensions are 10mmx10mm and ball pitch is 0.4mm.



	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	0.7	0.75	0.8
STAND OFF	A1	0	0.02	0.05
MOLD THICKNESS	A2	0.525	0.55	0.575
L/F THICKNESS	A3		0.203 REF	
LEAD WIDTH	b	0.15	0.2	0.25
BODY SIZE X	D		10 BSC	
BODY SIZE Y	E		10 BSC	
LEAD PITCH	e		0.4 BSC	
EP SIZE X	D2	5.5	5.6	5.7
EP SIZE Y	E2	5.63	5.73	5.83
LEAD LENGTH	L	0.275	0.35	0.425
LEAD TIP TO EXPOSED PAD EDGE	K		1.85 REF	
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	ccc		0.1	
COPLANARITY	eee		0.08	
LEAD OFFSET	bbb		0.07	
EXPOSED PAD OFFSET	fff		0.1	

NOTES:
1.REFER TO JEDEC MO-220;
2.COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD;
3.BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES;
4.FINISH: Cu/EP·Sn8~20s

Fig. 3-1 XS9922B Package Mechanical Data

3.1.2 PIN Map

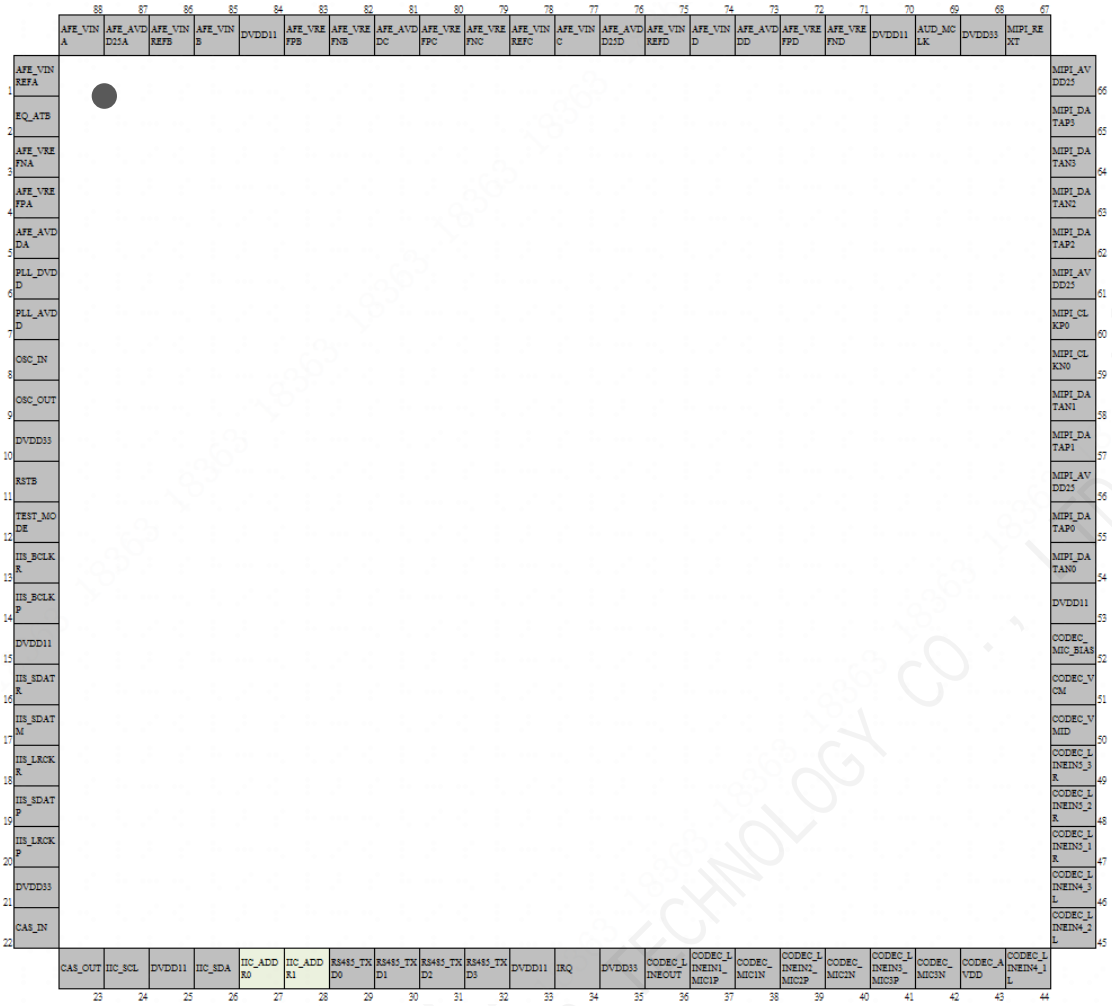


Fig. 3-2 XS9922B Pin Map

3.1.3 PIN Description

3.1.3.1 PIN Type

Table 3-1 XS9922B PIN Type Info

I/O	Description
I	Input
I_{PD}	Input, pull-down with 75KΩ
I_{PU}	Input, pull-up with 75KΩ
O	Output
I/O	Inout
I_{PD}/O	Inout, input with 75KΩ pull-down
I_{PU}/O	Inout, input with 75KΩ pull-up
A	Analog
P	Power

G	GND

3.1.3.2 Power/GND

Table 3-2 Power/GND PIN

Name	PIN No.	Type	Voltage（V）	Description
AFE_AVDD	5,73,81	P	1.1	AFE/EQ Analog Power 1.1V
AFE_AVDD25	76,87	P	2.5	AFE/EQ Analog Power 2.5V
CODEC_AVDD	43	P	3.3	Codec Analog Power
DVDD11	15,25,33,53,70,84	P	1.1	Digital Core Power 1.1V
DVDD33	10,21,35,68	P	3.3	Digital IO Power 3.3V
DVDD18	-	P	1.8	Digital IO Power 1.8V
AFE_AGND	-	G	-	AFE/EQ Analog GND
AFE_AGND25	-	G	-	AFE/EQ Analog GND
AVSS_CODEC	-	G	-	Codec Analog GND
DVSS	-	G	-	Digital GND
PLL_AVDD	7	P	2.5	PLL Analog Power
PLL_DVDD	6	P	1.1	PLL Digital Power
PLL_VSS	-	G	-	PLL GND

3.1.3.3 OSC

Table 3-3 OSC PIN

Name	PIN No.	Type	Driver（mA）	Voltage（V）	Description
OSC_IN	8	I	-	3.3	crystal Input or clock input, 27MHz
OSC_OUT	9	O	-	3.3	Crystal output

3.1.3.4 IIC

Table 3-4 IIC PIN

Name	PIN No.	Type	Driver（mA）	Voltage（V）	Description
IIC_SCL	24	I_{PU}	-	3.3	IIC Clock
IIC_SDA	26	I_{PU}/O	CFG	3.3	IIC Data
IIC_ADDR0	27	I	-	3.3	IIC Slave Address BIT0
IIC_ADDR1	28	I	-	3.3	IIC Slave Address BIT1

3.1.3.5 MIPI TX

Table 3-5 MIPI TX PIN

Name	PIN No.	Type	Driver（mA）	Voltage（V）	Description
MIPI0_CLKP0	60	A	-	2.5	MIPI0 Clock Lane Positive Output
MIPI0_CLKN0	59	A	-	2.5	MIPI0 Clock Lane Negative Output
MIPI0_DATAP0	55	A	-	2.5	MIPI0 Data Lane0 Positive Output
MIPI0_DATAN0	54	A	-	2.5	MIPI0 Data Lane0 Negative Output
MIPI0_DATAP1	57	A	-	2.5	MIPI0 Data Lane1 Positive Output
MIPI0_DATAN1	58	A	-	2.5	MIPI0 Data Lane1 Negative Output
MIPI0_DATAP2	62	A	-	2.5	MIPI0 Data Lane2 Positive Output
MIPI0_DATAN2	63	A	-	2.5	MIPI0 Data Lane2 Negative Output
MIPI0_DATAP3	65	A	-	2.5	MIPI0 Data Lane3 Positive Output
MIPI0_DATAN3	64	A	-	2.5	MIPI0 Data Lane3 Negative Output
MIPI0_REXT	67	A	-	2.5	MIPI0 Probing Pin（including REXTV Signal）
MIPI0_AGND	-	G	-	-	MIPI0 Analog GND
MIPI0_AVDD25	56,61,66	P	-	2.5	MIPI0 Analog Power

3.1.3.6 Audio

Table 3-6 Audio PIN

Name	PIN No.	Type	Driver（mA）	Voltage（V）	Description
IIS_BCLKP	14	I/O	CFG	3.3	PlayBack IIS Bit Clock
IIS_LRCKP	20	I/O	CFG	3.3	PlayBack IIS Bit Clock
IIS_SDATP	19	I	-	3.3	PlayBack IIS Data
IIS_BCLKR	13	I/O	CFG	3.3	Record IIS Bit Clock
IIS_LRCKR	18	I/O	CFG	3.3	Record IIS Bit Clock
IIS_SDATR	16	O	CFG	3.3	Record IIS Data
IIS_SDATM	17	O	CFG	3.3	Record IIS Data-M
CAS_IN	22	I	-	3.3	Audio Cascade Input
CAS_OUT	23	O	CFG	3.3	Audio Cascade Output
AUD_MCLK	69	I	-	3.3	Audio Master Clock Input

3.1.3.7 Analog Video

Table 3-7 Analog Video PIN

Name	PIN No.	Type	Voltage（V）	Description
AFE_VINA	88	A	2.5	Analog Video Signal Input CH0
AFE_VINREFA	1	A	2.5	Analog Video Signal Reference CH0
AFE_VINB	85	A	2.5	Analog Video Signal Input CH1
AFE_VINREFB	86	A	2.5	Analog Video Signal Reference CH1
AFE_VINC	77	A	2.5	Analog Video Signal Input CH2

AFE_VINREFC	78	A	2.5	Analog Video Signal Reference CH2
AFE_VIND	74	A	2.5	Analog Video Signal Input CH3
AFE_VINREFD	75	A	2.5	Analog Video Signal Reference CH3
AFE_VREFPA	4	A	1.1	CH0 Analog Reference Positive
AFE_VREFNA	3	A	1.1	CH0 Analog Reference Negative
AFE_VREFPB	83	A	1.1	CH1 Analog Reference Positive
AFE_VREFNB	82	A	1.1	CH1 Analog Reference Negative
AFE_VREFPC	80	A	1.1	CH2 Analog Reference Positive
AFE_VREFNC	79	A	1.1	CH2 Analog Reference Negative
AFE_VREFPD	72	A	1.1	CH3 Analog Reference Positive
AFE_VREFND	71	A	1.1	CH3 Analog Reference Negative
EQ_ATB	2	A	2.5	EQ Test Output

3.1.3.8 Audio Codec

Table 3-8 Audio Codec PIN

Name	PIN No.	Type	Voltage（V）	Description
CODEC_LINEIN1_MIC1P	37	A	3.3	Audio Codec CH1 LineIn1 / MIC1P
CODEC_MIC1N	38	A	3.3	Audio Codec CH1 MIC1N
CODEC_LINEIN2_MIC2P	39	A	3.3	Audio Codec CH2 LineIn2 / MIC2P
CODEC_MIC2N	40	A	3.3	Audio Codec CH2 MIC2N
CODEC_LINEIN3_MIC2P	41	A	3.3	Audio Codec CH3 LineIn3 / MIC3P
CODEC_MIC3N	42	A	3.3	Audio Codec CH3 MIC3N
CODEC_LINEIN4_1L	44	A	3.3	Audio Codec CH4 LineIn 1
CODEC_LINEIN4_2L	45	A	3.3	Audio Codec CH4 LineIn 2
CODEC_LINEIN4_3L	46	A	3.3	Audio Codec CH4 LineIn 3
CODEC_LINEIN5_1R	47	A	3.3	Audio Codec CH5 LineIn 1
CODEC_LINEIN5_2R	48	A	3.3	Audio Codec CH5 LineIn 2
CODEC_LINEIN5_3R	49	A	3.3	Audio Codec CH5 LineIn 3
CODEC_LINEOUT	36	A	3.3	Audio Codec LineOut
CODEC_VMID	50	A	3.3	Audio Codec VMID
CODEC_VCM	51	A	3.3	Audio Codec VCM
CODEC_MIC_BIAS	52	A	3.3	Audio Codec MIC BIAS Output

3.1.3.9 SYS

Table 3-9 SYS PIN

Name	PIN No.	Type	Driver（mA）	Voltage（V）	Description
RSTB	11	I_{PU}	-	3.3	System Reset (Active low)
TEST_MODE	12	I_{PD}	-	3.3	Test Mode Selection PIN (Normally connect to GND)

IRQ	34	O	CFG	3.3	Interrupt Output, level triggered, configurable polarity

3.1.3.10 Others

Table 3-10 Other PIN

Name	PIN No.	Type	Driver（mA）	Voltage（V）	Description
RS485_TXD0	29	O	CFG	3.3	CH0 PTZ Output
RS485_TXD1	30	O	CFG	3.3	CH1 PTZ Output
RS485_TXD2	31	O	CFG	3.3	CH2 PTZ Output
RS485_TXD3	32	O	CFG	3.3	CH3 PTZ Output

3.1.4 Multiplexed PIN

Table 3-11 Multiplexed PIN Description

TEST_MODE	IIC_ADDR1	IIC_ADDR0	Mode
1	1	1	Debug Mode
1	1	0	DFT Mode
0	X	X	Function Mode

3.2 Electrical Specifications

3.2.1 Power Consumption

Table 3-12 XS9922B Power Consumption

Symbol	Parameter	Min	Typ	Max	Unit
DVDD33	Digital IO Power (3.3V)	-	9	-	mA
DVDD11 & PLL_DVDD	Digital core Power (1.1V)	-	165	-	mA
AFE_AVDD25 & PLL_AVDD	Analog Power (AFE 2.5V)	-	79	-	mA
CODEC_AVDD	Analog Power (Codec 3.3V)	-	16	-	mA
AFE_AVDD	Analog Power (AFE 1.1V)	-	76	-	mA
MIPI_AVDD25	Analog Power (MIPI 2.5V)	-	14	-	mA

3.2.2 Temperature and Thermal Resistance

Table 3-13 XS9922B(QFN88) Temperature Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_A	Ambient Temperature	0	-	85	℃
T_J	Junction Temperature	-40	-	110	℃

Table 3-14 XS9922B(QFN88) Thermal Resistance Characteristics @4 Layers PCB

Symbol	Parameter	Min	Typ	Max	Unit
θ_{JA}	Junction-to-ambient	-	26.875	-	℃/W
θ_{JB}	Junction-to-board	-	8.25	-	℃/W
θ_{JC}	Junction-to-case	-	3.625	-	℃/W
Psi_{Jt}	Junction temp.-Package top temp	-	0.25	-	℃/W
Psi_{Jb}	Junction temp.-Board temp	-	3.125	-	℃/W

Note:

- Thermal Resistance is based on JEDEC JESD51-9 standard. Please do actual analysis according to different ambient, system design and application conditions.
- Chip power consumption is proportional to junction temperature, please control the junction temperature within a reasonable range when system design.

3.2.3 Recommended Operating Conditions

Table 3-15 describes the recommended operating conditions of XS9922B.

Table 3-15 XS9922B Operating Conditions

PIN	Description	Min	Typ	Max	Unit
AFE_AVDD	AFE Analog Power 1.1V	1.045	1.1	1.155	V

AFE_AVDD25	AFE Analog Power 2.5V	2.275	2.5	2.75	V
CODEC AVDD	Codec Analog Power 3.3V	2.97	3.3	3.63	V
MIPI_AVDD25	MIPI Analog Power 2.5V	2.275	2.5	2.75	V
DVDD11	Digital Core Power	1.045	1.1	1.155	V
DVDD33	Digital IO Power	2.97	3.3	3.63	V
PLL_AVDD	PLL Analog Power	2.375	2.5	2.625	V
PLL_DVDD	PLL Digital Power	1.045	1.1	1.155	V

3.2.4 Sequence of Power-On and Power-Off

To avoid overcurrent of I/O pins during power-on, recommend to power on DVDD33 and DVDD11 in sequence. There is no requirement for the sequence of power-off.

3.2.5 DC/AC Electrical Specification

Table 3-16 XS9922B DC Electrical Specification (DVDD33=3.3V)

Symbol	Parameter	Min	Typ	Max	Unit	Note
DVDD33	3.3V Interface Voltage	2.97	3.3	3.63	V	
V_{IL}	Input Low Voltage	-	-	0.8	V	LVTTL
V_{IH}	Input High Voltage	2.0	-	-	V	LVTTL
V_{OL}	Output Low Voltage	-	-	0.4	V	I_{ol} = 4.0 mA ~ 16 mA
V_{OH}	Output High Voltage	2.4	-	-	V	I_{oh} = 4.0 mA ~ 16 mA
R_{PU}	Internal Pull-up Resistor	40	75	190	kΩ	V_{in} = 0 V
R_{PD}	Internal Pull-down Resistor	30	75	190	kΩ	V_{in} = DVDD33
I_L	Input Leakage Current	-	±1.0	±10.0	μA	V_{in} = DVDD33 or 0 V
I_{OZ}	Tristate Output Leakage Current	-	±1.0	±10.0	μA	-

3.2.6 MIPI TX Electrical Specification

Please refer Specification for D-PHY Version 1.2 from MIPI Alliance.

3.3 Interface Timing

3.3.1 IIC Timing

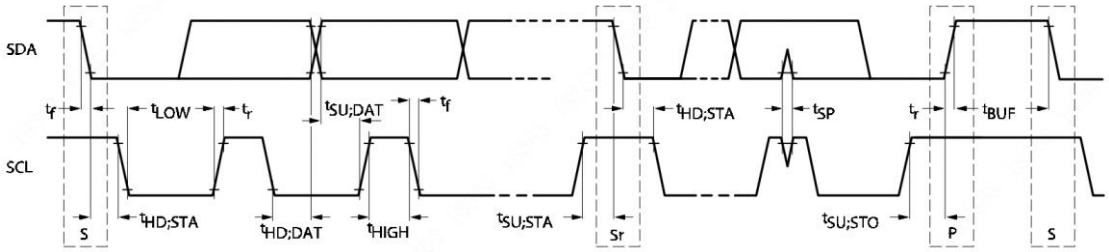


Fig. 3-3 IIC Timing

Table 3-17 IIC Timing Characteristics

Parameter	Symbol	Normal Mode		Fast Mode		Unit
		Min	Max	Min	Max	
Serial Clock Frequency	f_{SCL}	0	100	0	400	kHz
Start Hold Time	t_{HD}	4.0	-	0.6	-	μs
SCL Low-level Cycle	t_{LOW}	4.7	-	1.3	-	μs
SCL High-level Cycle	t_{HIGH}	4.0	-	0.6	-	μs
Start Setup Time	$t_{SU;STA}$	4.7	--	0.6	-	μs
Data Hold Time	$t_{HD;DAT}$	0	3.45	0	0.9	μs
Data Setup Time	$t_{SU;DAT}$	250	-	100	-	ns
SDA and SCL Rising Time	t_r	-	1000	20+0.1C_b	300	ns
SDA and SCL Falling Time	t_f	-	300	20+0.1C_b	300	ns
End Setup Time	$t_{SU;STO}$	4.0	-	0.6	-	μs
Bus Release Time from Start to End	t_{BUF}	4.7	-	1.3	-	μs
Bus Load	C_b	-	400	-	400	pF

4 Function Description

4.1 System

4.1.1 Reset

The reset management module resets the entire chip and all functional modules.

- Manages power-on reset with 100ms reset time
- Controls the system soft reset and the functional module soft reset
- Synchronizes reset signals to the clock domain corresponding to each module

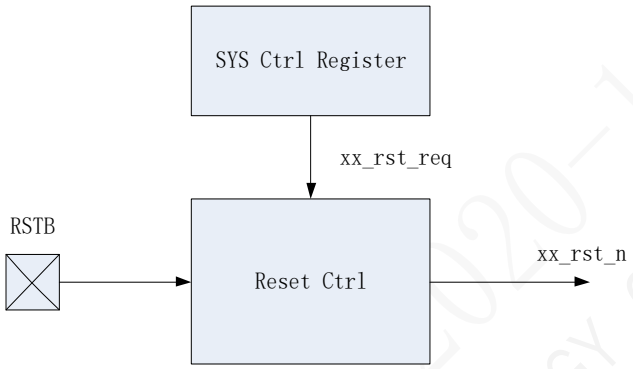


Fig.4-1 Reset controller

Note:

- RSTB: power-on reset signal, derived from RSTB pin.
- xx_rst_n: separate soft reset signals of each functional module.

4.1.2 Clock

The clock management module manages clock input, clock generation, and clock control in a unified manner.

- 27MHz input clock
- Clock frequencies generating and controlling
- Clock Gating
- Clock Delay Line

Table 4-1 Clock Input

Parameter	Symbol	Min	Typ	Max	Unit
Nominal Frequency		-	27	-	MHz
Frequency Deviation		-25	-	25	ppm

4.1.3 Interrupt

XS9922B supports 3 types of interrupts as below. The interrupts can be masked, or cleared by configuring the corresponding interrupt registers.

- Video loss interrupts for 4 channels
- Remote communication interrupts for 4 channels
- MIPI interrupts

4.1.4 IIC

XS9922B provides a IIC slave interface.

- 100Kbps < speed < 400Kbps
- Configurable 2Bit for slave address
- Support single read/write and continuous read/write for fixed address

4.1.4.1 IIC Slave Address Configuration

Table 4-2 XS9922B IIC Slave Address

IIC_ADDR1	IIC_ADDR0	Slave Address
Pull_Down	Pull_Down	0x60
Pull_Down	Pull_Up	0x62
Pull_Up	Pull_Down	0x64
Pull_Up	Pull_Up	0x66

4.1.4.2 IIC read/write operation protocol

The following is IIC read/write operation protocol of 16bit address.

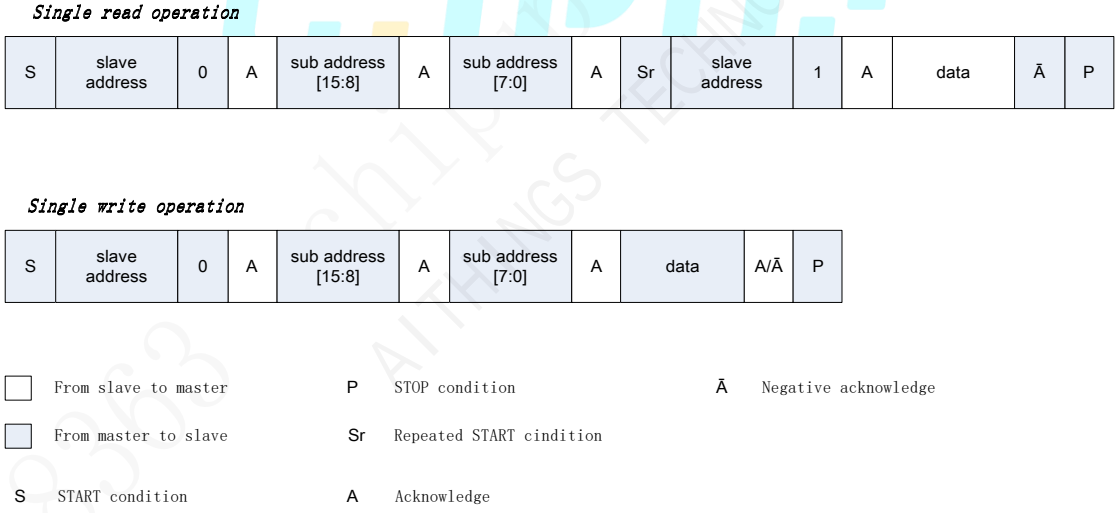


Fig.4-2 IIC read/write operation protocol (16Bit address)

4.2 Video Processing

4.2.1 Video Detection

XS9922B provides the robust video detection. It firstly judges whether the video signal is HD video signal or SD video signal, then detects and locks the video format of HD/SD video signal. The following diagram shows video detection flow.

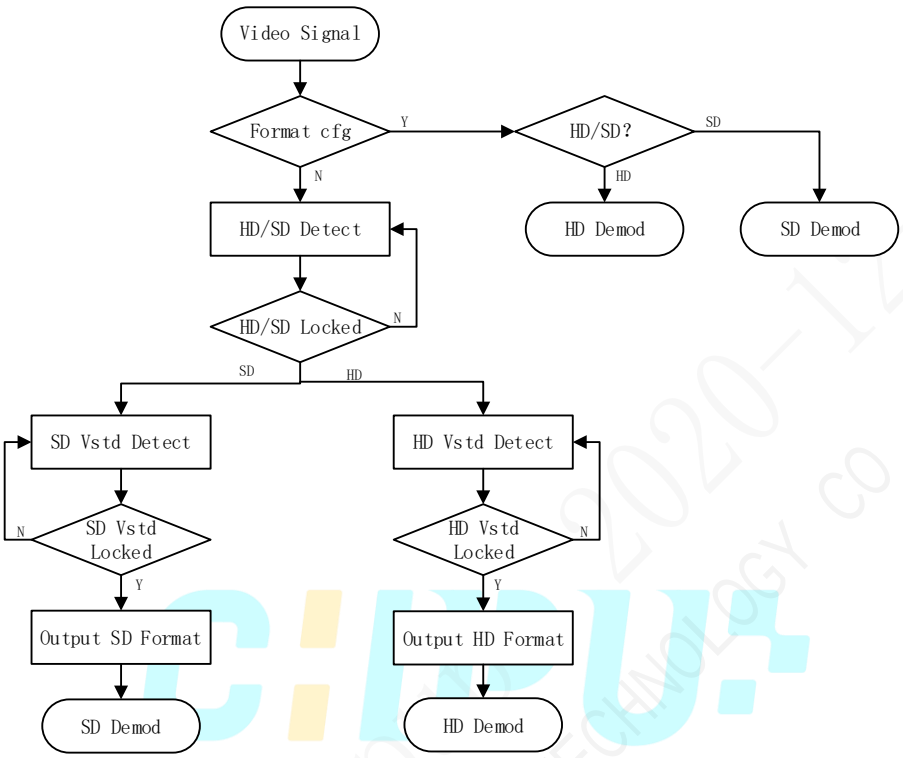


Fig.4-3 Video Detection Flow

4.2.2 Video Signal Sync

XS9922B provides the robust video signal synchronizing circuits. The circuits can realize horizontal sync, vertical sync, and color subcarrier sync.

4.2.3 Y/C Separation and Demodulation

The high-performance Y/C separation filter is used to separate the luminance and chrominance components from the composite video signal. This is achieved by low-pass filter, band-pass filter and comb filter. XS9922B also provides peaking filter and gain control for emphasizing or depressing the high-frequency region.

The chroma processing mainly consists three parts: demodulation, filtering and ACC (Automatic Chroma-gain Control). The chroma demodulator receives modulated chroma signal for Y/C separator, and generates demodulated U and V data. ACC can compensate for reduced amplitudes caused by high-frequency loss in video signal.

4.2.4 Component Processing

XS9922B supports the typical brightness, contrast, color saturation and hue adjustment for changing the output video characteristic.

XS9922B supports color killer. The color will be “killed” for easy viewing for low color amplitude signals, black and white video, or noisy signals.

4.2.5 Frequency Offset Compensation

The color subcarrier frequency offset compensation solves color deviation in the horizontal direction. The following diagram shows the effect of frequency offset compensation.

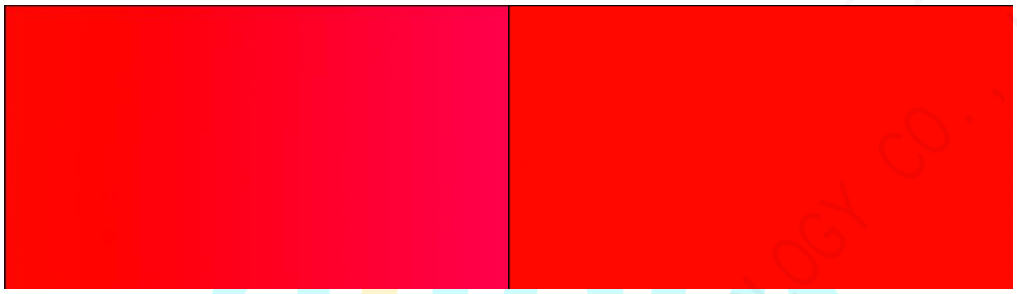


Fig.4-4 Image Effect of Pre-compensation(L) VS Post-compensation(R)

4.3 Video Output

XS9922B supports a 4*Lane MIPI interface compliant with MIPI CSI-2 V1.2 and D-PHY V1.1 spec. The max data rate of MIPI data lane is up to 1.5Gbps with YUV422 8bit format.

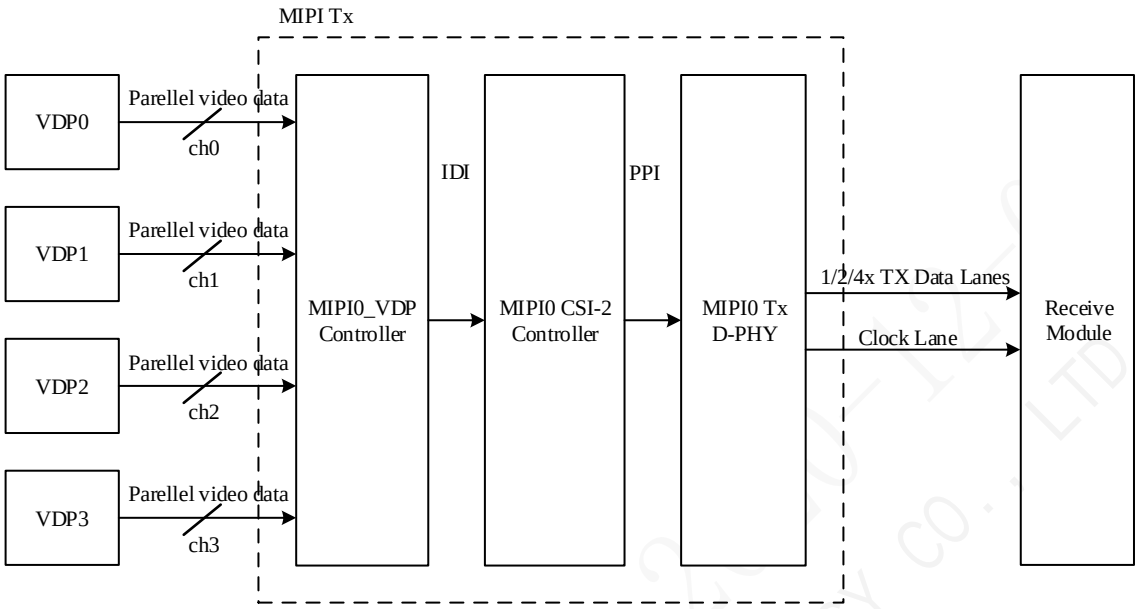


Fig. 4-5 MIPI TX System Diagram

4.3.1 MIPI Frame Packet Format

MIPI CSI image frame packet contains FS(Frame Start), FE(Frame End), PH(Packet Header), PF(Packet Footer) and DATA. The frame packet format is illustrated in the following figure.

Fig. 4-6 MIPI Frame Packet Format

The following diagram shows the image frame packet format in 4 data lanes.

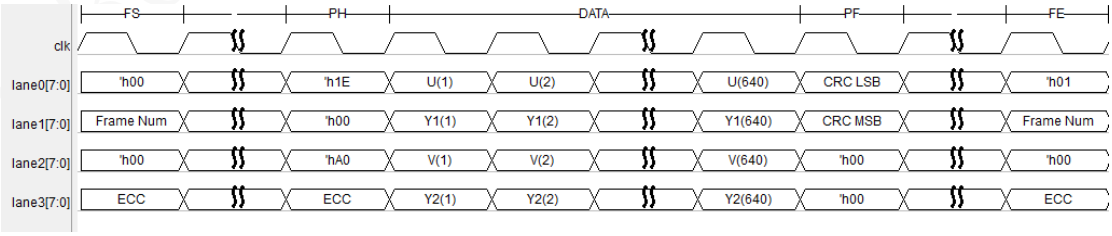


Fig. 4-7 Frame Packet Format in 4 Data Lanes

The detailed information of each data lane for different packet components is illustrated in the following table.

The frm_num specifies video frame number, which can be used to distinguish video parity fields when transmitting CVBS.

The word_count specifies size of the payload data. If the video data format is YUV422, the word_count equal to twice the number of pixels in a line.

Table 4-3 Detailed Information of Each Lane in Frame Packet

	lane0[7:0]	lane1[7:0]	lane2[7:0]	lane3[7:0]
FS	data_id[7:0]	{5'h0,frm_num[2:0]}	8'h00	ECC_code[7:0]
FE	data_id[7:0]	{5'h0,frm_num[2:0]}	8'h00	ECC_code[7:0]
PH	data_id[7:0]	word_count[7:0]	word_count[15:8]	ECC_code[7:0]
PF	CRC_code[7:0]	CRC_code[15:8]	8'h00	8'h00
DATA	U[7:0]	Y1[7:0]	V[7:0]	Y2[7:0]

4.3.2 Data Identifier(data_id)

The Data Identifier byte contains Virtual Channel Identifier value and Data Type value as illustrated in the following figure.

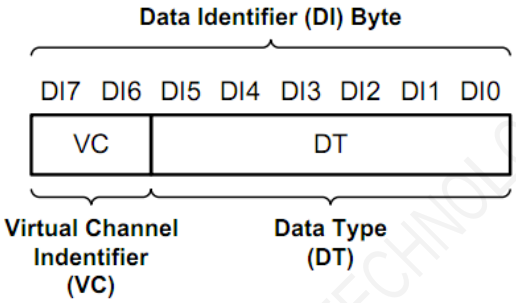


Fig.4-8 data_id(Data Identifier)

The Virtual Channel Identifier allows different data within a single data stream to be logically separated from each other. Each virtual channel has its own Frame Start and Frame End package. Therefore, it is possible for different virtual channels to have different frame rates.

Receivers should be able to de-multiplex different frames of image data based on the Virtual Channel Identifier. For example, the Virtual Channel Identifier value of CH0 video data is 0, and the Virtual Channel Identifier value of CH1 video data is 1.

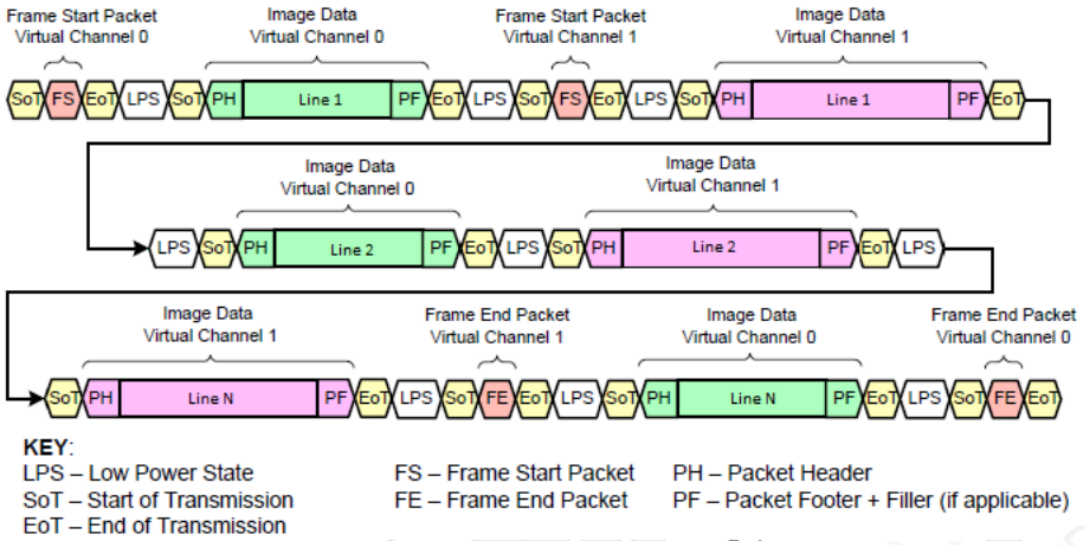


Fig. 4-9 Interleaved data Transmission using Virtual Channels

The Data Type value specifies the format and content of the payload data.

Table 4-4 Data Type Classes

Data Type[5:0]	Description
0x00	Frame Start Code
0x01	Frame End Code
0x1E	YUV422 8-bit

4.3.3 SD Video Frame Transmission

SD video frame consists of odd filed and even field. The frm_num is used to identify the type of field when SD video frame transmission.

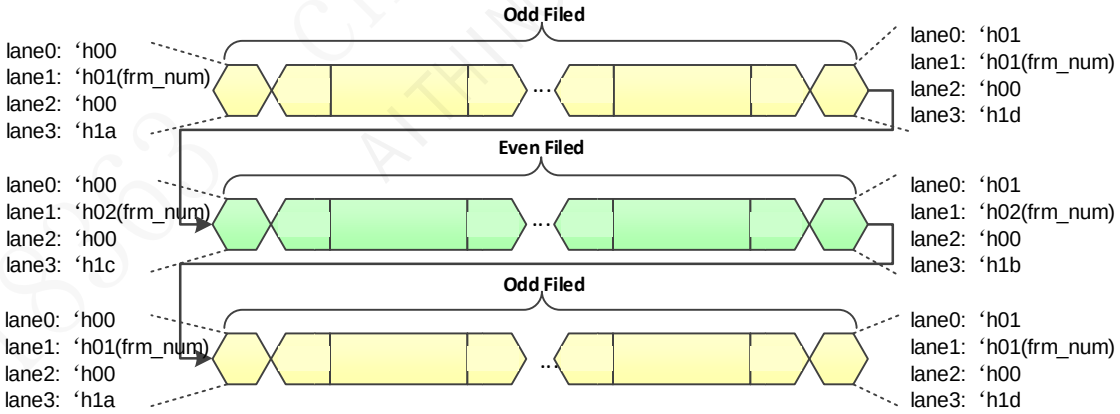


Fig. 4-10 SD Video Frame Format

4.3.4 Video Multiplex Transmission

MIPI CSI-2 supports video multiplex transmission using virtual channels. XS9922B supports Max 4 Virtual Channels.

Normal application modes are as below:

- 4 Data Lane for up to 1080p@30 4-CH
- 2 Data Lane for up to 1080p@30 2-CH
- 2 Data Lane for up to 1080p@30 1-CH and 720p@30 2-CH
- 1 Data Lane for up to 1080p@30 1-CH
- 1 Data Lane for up to 720p@30 2-CH

4.3.5 1/2/3/4 Lane Mode

XS9922B supports 1*Lane, 2*Lane, 3*Lane and 4*Lane mode. The following four diagrams show data transmission of different lane mode.

Fig. 4-11 MIPI 1*Lane Data Transmission Mode

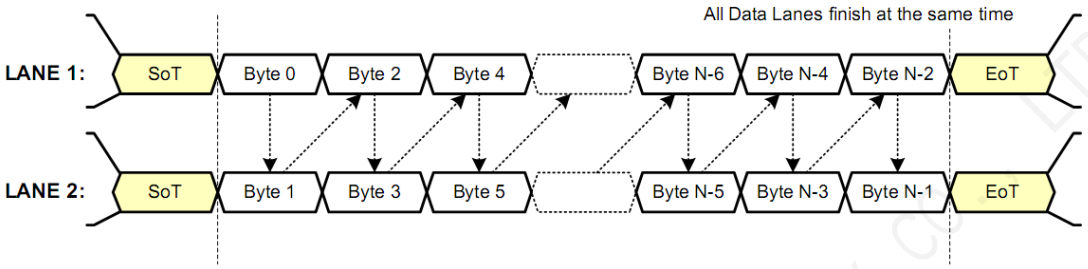


Fig. 4-12 MIPI 2*Lane Data Transmission Mode

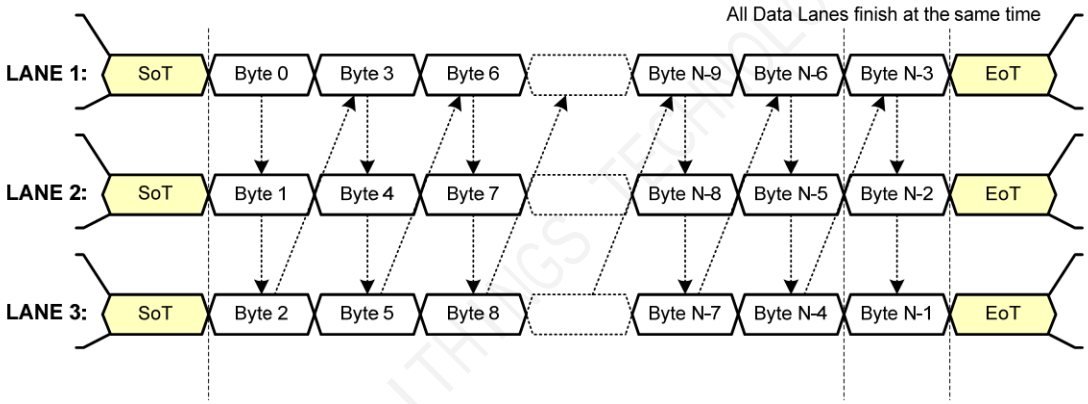


Fig. 4-13 MIPI 3*Lane Data Transmission Mode

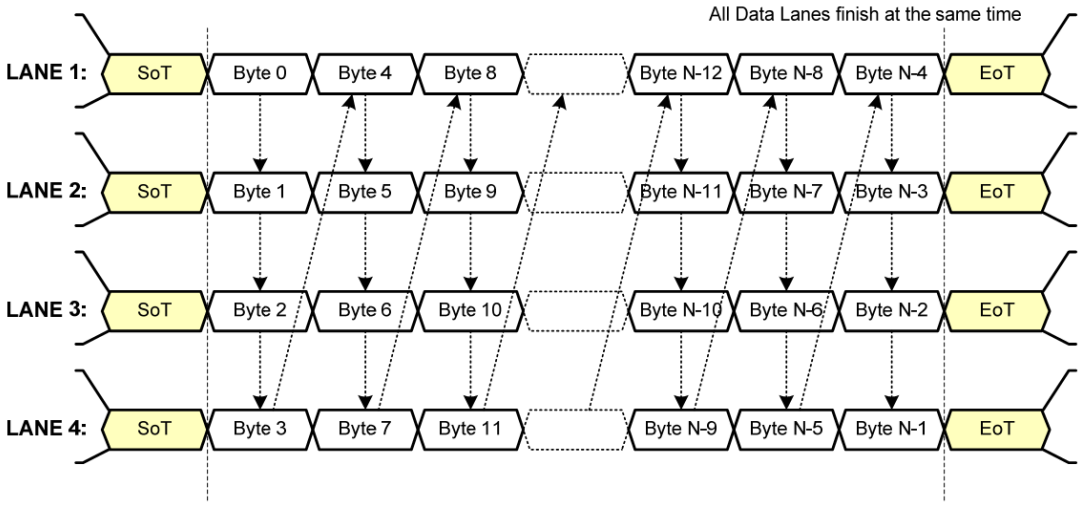


Fig.4-14 MIPI 4*Lane Data Transmission Mode

4.4 Audio

XS9922B samples audio transmission via coaxial cable (“Coaxial Audio”) or Local Audio (form Audio Codec), and output audio data through IIS interface. Also, XS9922B supports sample audio data from IIS interface and output through Audio Codec LineOut.

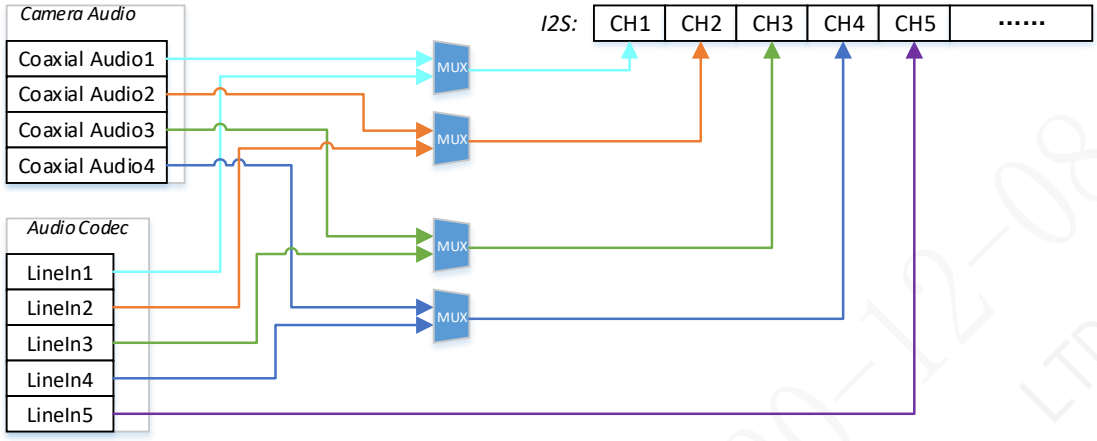


Fig. 4-15 Audio Data Sample and Output Path

4.4.1 Coaxial Audio

XS9922B supports audio transmission via coaxial cable (“Coaxial Audio”). It samples and decodes audio signal from remote camera device. It supports 16-bit/8KHz, 16-bit/16KHz sample rate.

4.4.2 Local Audio

XS9922B integrates high-performance Audio Codec, which includes 3-CH LineIn/MIC, 2-CH LineIn, and 1-CH LineOut. The Audio Codec supports 8K/16K/32K/44.1K/48K sample rate, and 16/20/24bit sample accuracy.

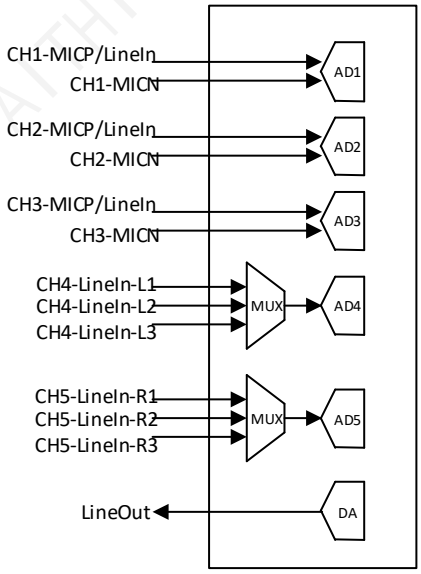


Fig. 4-16 Local Audio Codec Interface

4.4.3 IIS

XS9922B embeds 2-CH IIS interface, one for audio recorder, the other for audio playback. IIS supports 8K/16K/32K/44.1K/48K sample rate, and 16/20/24bit sample accuracy. IIS interface cooperates with audio decoder chip to complete voice recording and playing. IIS Interface supports the master/salve mode.

Note:

- In slave mode, IIS only supports 8K/16K/32K sample rate.
- In slave mode, don't support the data path from IIS to Audio Codec LineOut.
- In TDM Mode1, IIS sample accuracy supports 16bit. In TDM Mode2, IIS sample accuracy supports 16/20/24bit.

4.4.3.1 IIS Output

IIS output interface contains IIS_BCLKR, IIS_LRCKR and IIS_SDATR/M.

TDM Mode1

IIS can send up to 16 channels 16-bit audio data in TDM Mode1.

- Audio Codec LineIn CH1~4 or Coaxial CH0~3 audio data can output via IIS_SDATR.
- Audio Codec LineIn CH5 audio data can output via IIS_SDATM.

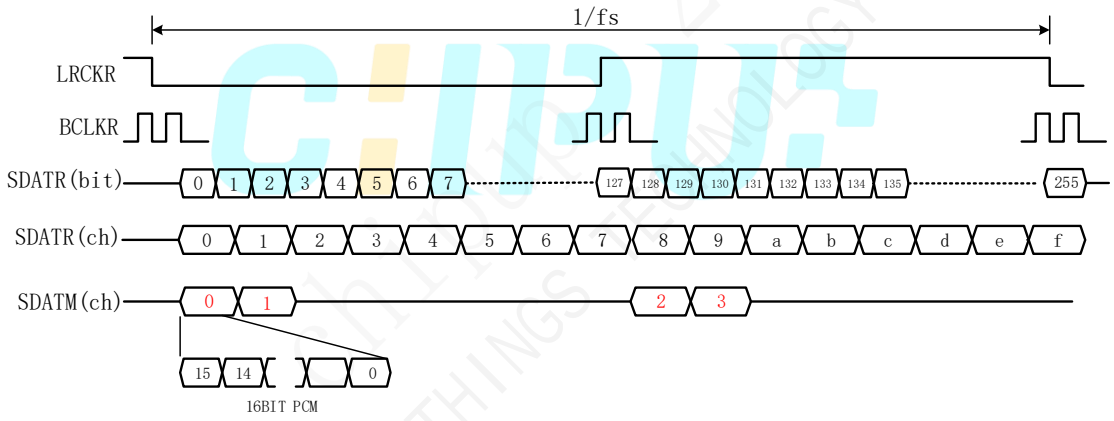


Fig.4-17 TDM Mode1 IIS Format Output Timing

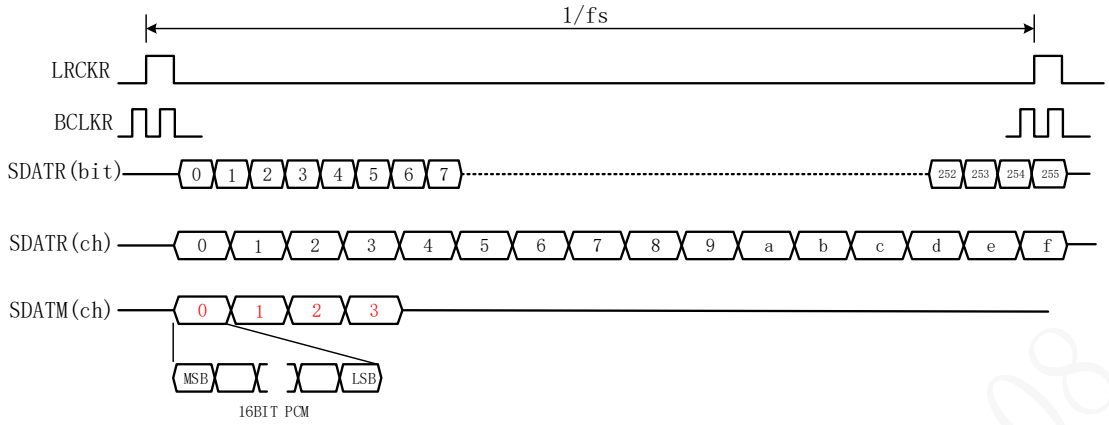


Fig. 4-18 TDM Mode1 DSP Format Output Timing

TDM Mode2

IIS can send up to 8 channels 16/20/24bit audio data in TDM Mode2.

- Audio Codec LineIn CH1~5 or Coaxial CH0~3 audio data can output via IIS_SDATR/M.

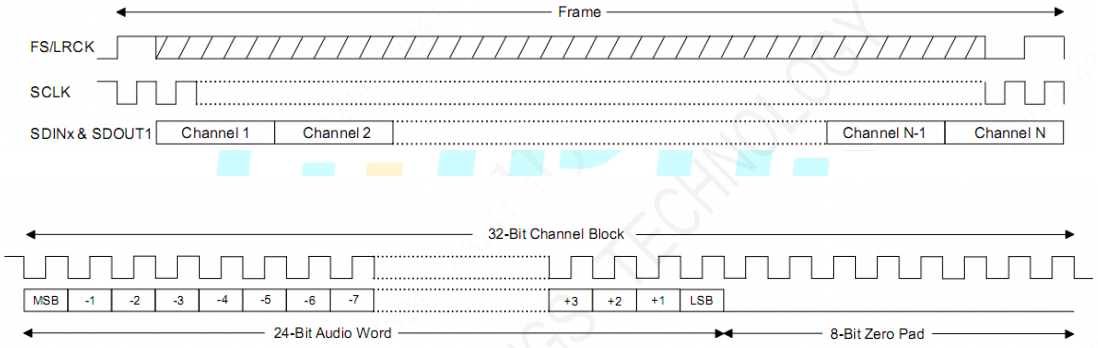


Fig. 4-19 TDM Mode2 DSP Format Output Timing

4.4.3.2 IIS Input

IIS input interface contains IIS_BCLKP, IIS_LRCKP and IIS_SDATP. IIS input only supports single channel audio data. It receives left-/right-channel 16-/20-/24-bit data.

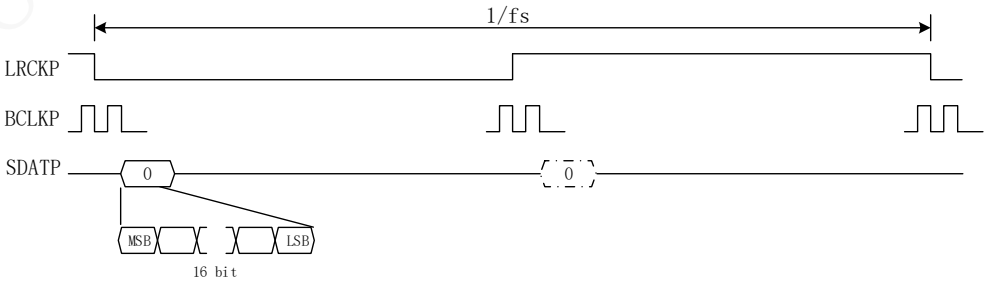


Fig. 4-20 IIS Format Input Timing

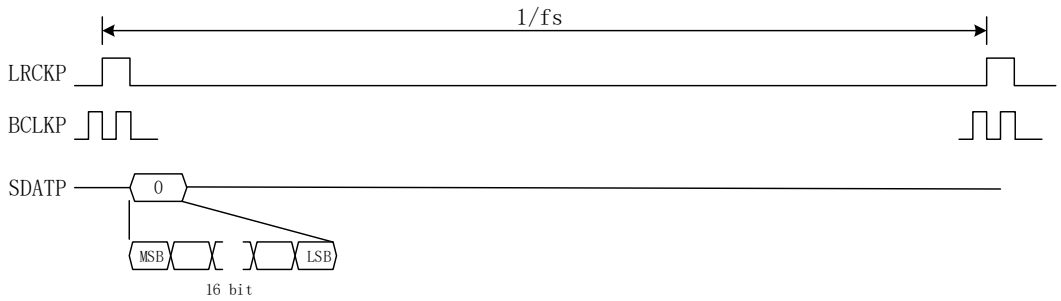


Fig.4-21 DSP Format Input Timing

4.4.4 Audio Cascade

XS9922B audio cascade supports up to max 4 chips. The following diagram shows the audio cascade between four XS9922B chips. Each chip contains an ID number for audio cascade. The ID number of first stage chip is 0, and the last stage chip is 3.

- Each chip supports up to 5 audio channels.
- First stage chip can receive up to 20 audio channels.
- AIN1~AIN16 audio data is from Coaxial Audio or Local Audio.
- AIN51~AIN54 audio data is from Local Audio.
- LineOut can output anyone of 20 audio channels.

Note:
Audio Cascade only supports 8K/16K/32K sample rate.

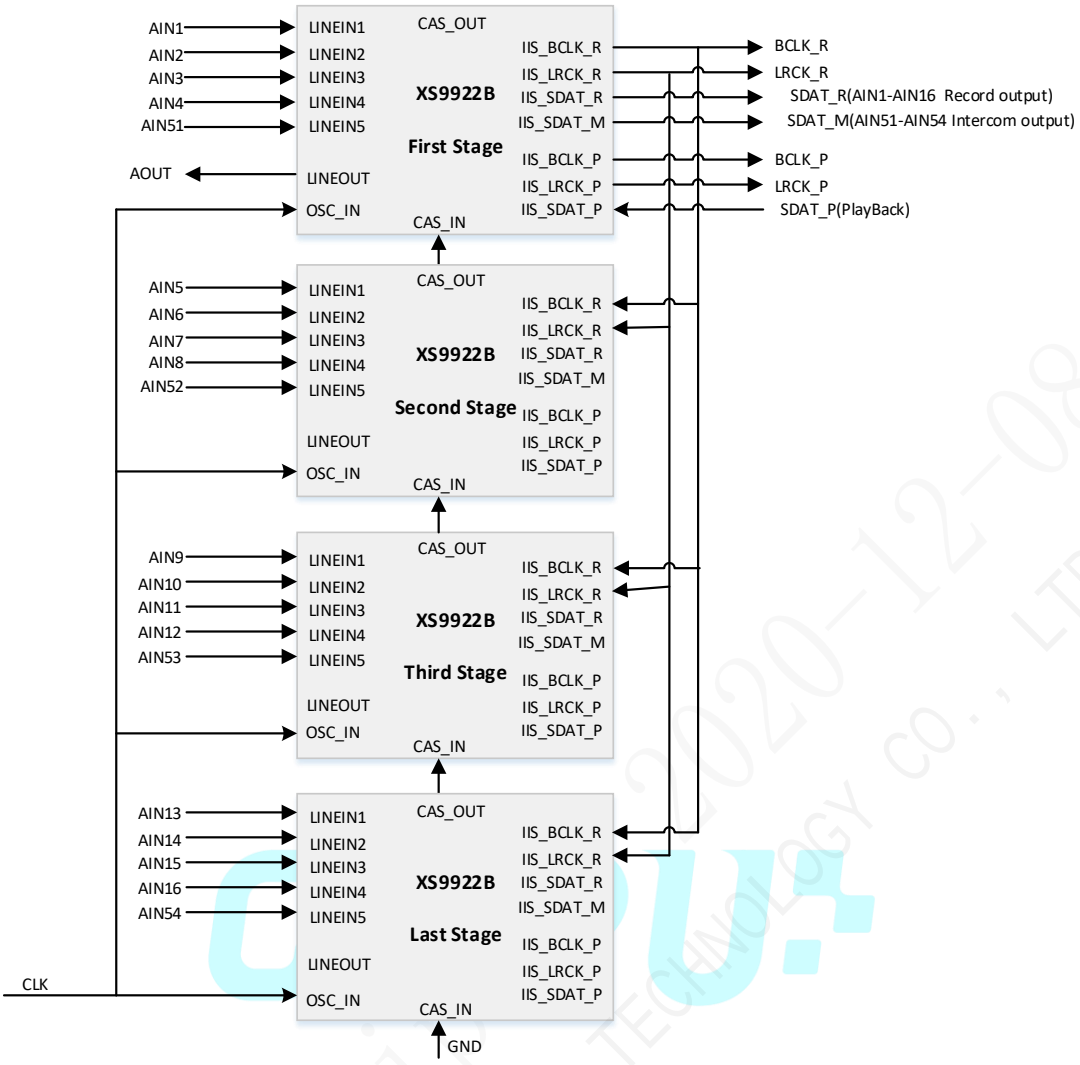


Fig.4-22 Audio Cascade between 4 chips

4.4.5 Audio Application Note

4.4.5.1 4-CH LineIn@2-chips Cascade

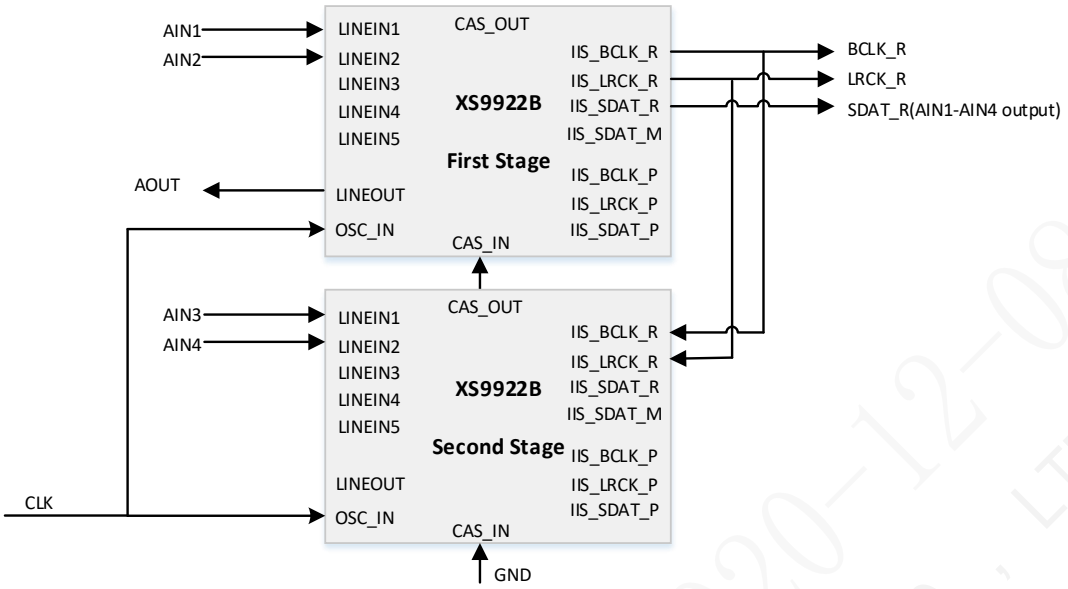


Fig. 4-23 4-CH LineIn@2-chips Cascade Connection

The IIS interface output timing (IIS format) of 4-CH LineIn@2-chips Cascade mode is illustrated in the following diagram. Audio data of CH1/2/3/4 in SDATR bus corresponds to AIN1/AIN2/AIN3/AIN4.

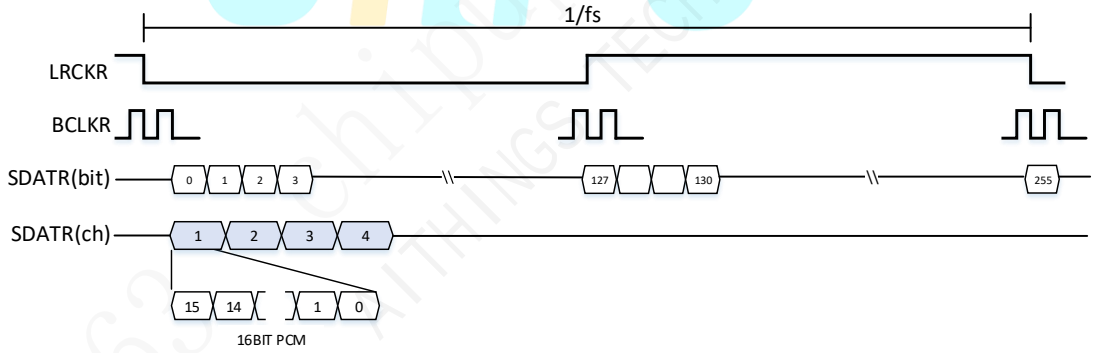


Fig. 4-24 IIS Timing of 4-CH LineIn@2-chips Cascade mode

4.4.5.2 4-CH LineIn@Local Audio

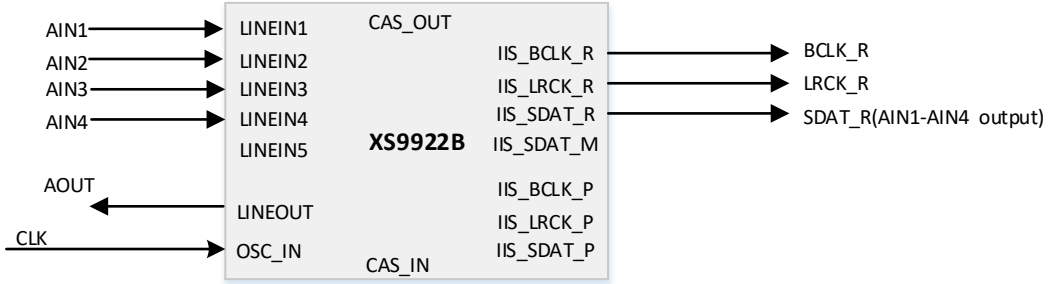


Fig. 4-25 4-CH LineIn@Local Audio Connection

The IIS interface output timing (IIS format) of 4-CH LineIn@Local Audio mode is illustrated in the following diagram. Audio data of CH1/2/3/4 in SDATR bus corresponds to AIN1/AIN2/AIN3/AIN4.

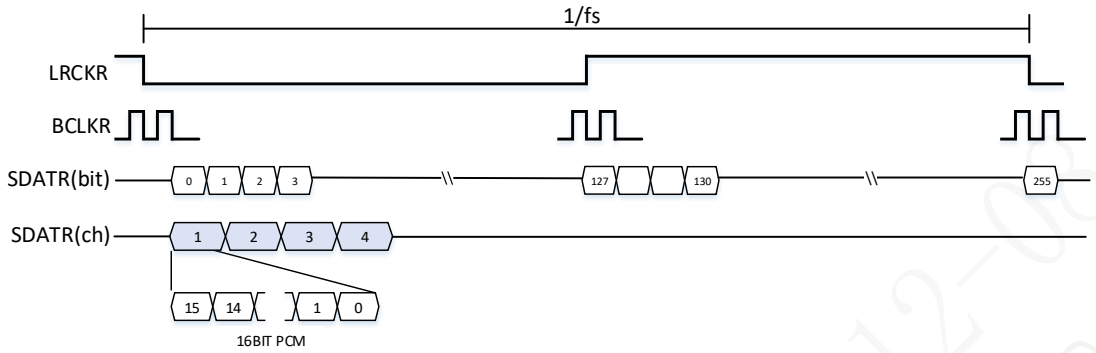


Fig. 4-26 IIS Timing of 4-CH LineIn@Local Audio mode

4.4.5.3 5-CH LineIn@Local Audio

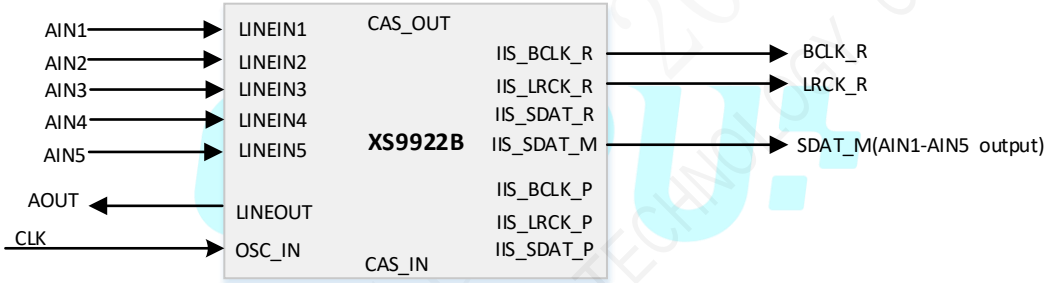


Fig. 4-27 5-CH LineIn@Local Audio Connection

The IIS interface output timing (DSP format) of 5-CH LineIn@Local Audio mode is illustrated in the following diagram. Audio data of CH1/2/3/4/5 in SDATM bus corresponds to AIN1/AIN2/AIN3/AIN4/AIN5.

The audio data outputs in TDM Mode2. Audio data is 32-bit for each channel. The MSB (bit[31:16]) is valid audio data and LSB (bit[15:0]) is invalid('0') when the audio data sample accuracy is 16*bit.

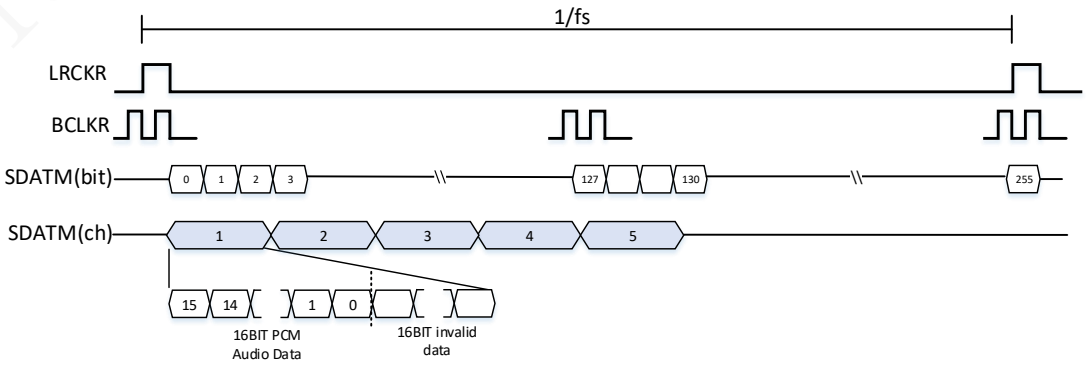


Fig. 4-28 IIS Timing of 5-CH LineIn@Local Audio mode

4.4.5.4 LineOut Stereo Output

2 chips receive left-/right-channel audio data via IIS input interface, and output stereo audio via Audio Codec LineOut. The following diagram shows the connection for this application mode.

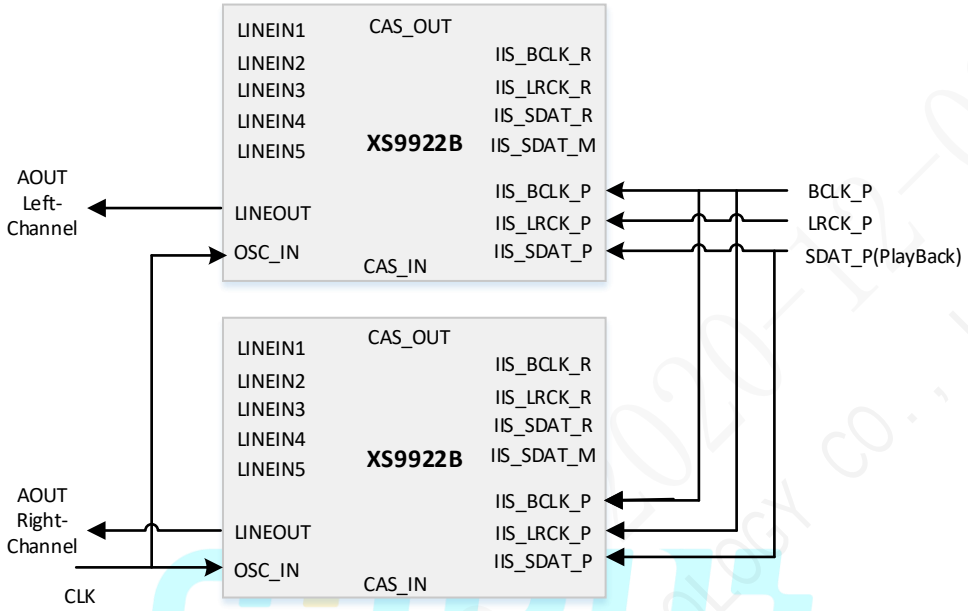


Fig. 4-29 LineOut Stereo Output@2-chips Connection

4.5 Coaxial Communication

XS9922B supports Coaxial Communication Protocol to communicate between DVR and Camera on the video signal via coaxial cable. XS9922B supports protocol for CVBS and HDCCTV.

XS9922B includes Coaxial Protocol generator that sends control command data to a pan and tilt, camera and lens on the video signal. And XS9922 integrates Coaxial Protocol decoder that receives command or Ack data from a pan and tilt, camera and lens on the video signal.

The coaxial communication data is sent within VBI lines as illustrated in the following diagrams.

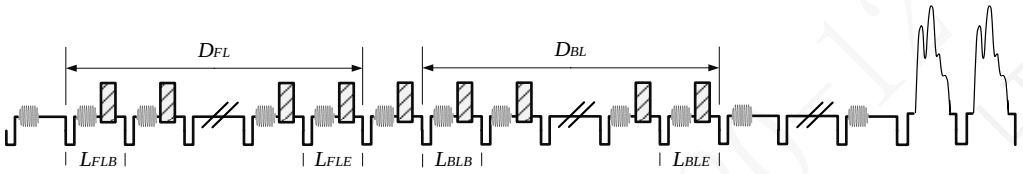


Fig. 4-30 Froward(DFL)/Backward(DBL) Communication on VBI

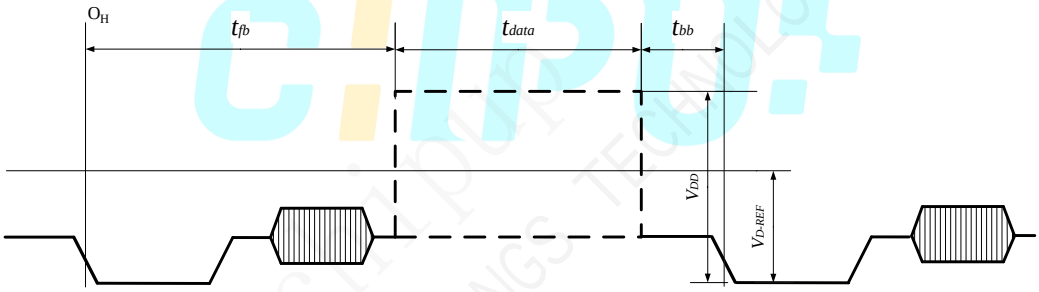


Fig. 4-31 Communication Protocol Data on VBI Line

4.6 AFE

XS9922B integrates high-performance AFE which contains ADC, EQ, and Cable Detector. The AFE supports 1.2Vpp analog signal input.

- The high speed 12-bit ADC is used for 2X over-sampling of analog video signal.
- EQ compensates the attenuation and group delay of video signal via long cable. The effect of EQ is illustrated in the following diagram.
- Cable Detector can detect whether the cable is connected or not. XS9922B can close clocks of the corresponding channel to reduce power consumption when the cable is not connected.

Fig.4-32 EQ Effect

5 Hardware Development Reference

Please refer the document: XS9922B Hardware Design User Guide.

A Acronyms and Abbreviations

A

ACC	Automatic Chroma Gain Control
AFE	Analogue Front End
AGC	Automatic Gain Control

C

CTI	Color Transient Improvement
CVBS	Composite Video Broadcast Signal
CSI	Camera Serial Interface

E

EQ	Equalizer

H

HDCVI	High Definition Composite Video Interface

I

IIC	Inter-Integrated Circuit
IIS	Inter-IC Sound

M

MIPI	Mobile Industry Processor Interface alliance

B Video Resolution

Table A-1 Video Resolution

	Resolution	Aspect Ratio	Frame Rate	Active Pixel / Line	Active Line / Frame
HDCCTV	1080p	16:9	30	1920	1080
	1080p	16:9	25	1920	1080
	720p	16:9	60	1280	720
	720p	16:9	50	1280	720
	720P	16:9	30	1280	720
	720P	16:9	25	1280	720
CVBS	960H_PAL		25	960	576
	960H_NTSC		30	960	480
	D1_PAL		25	720	576
	D1_NTSC		30	720	480